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Detecting Asymmetries within Multi-Chip SiC Power Modules by Means of the Kelvin Source

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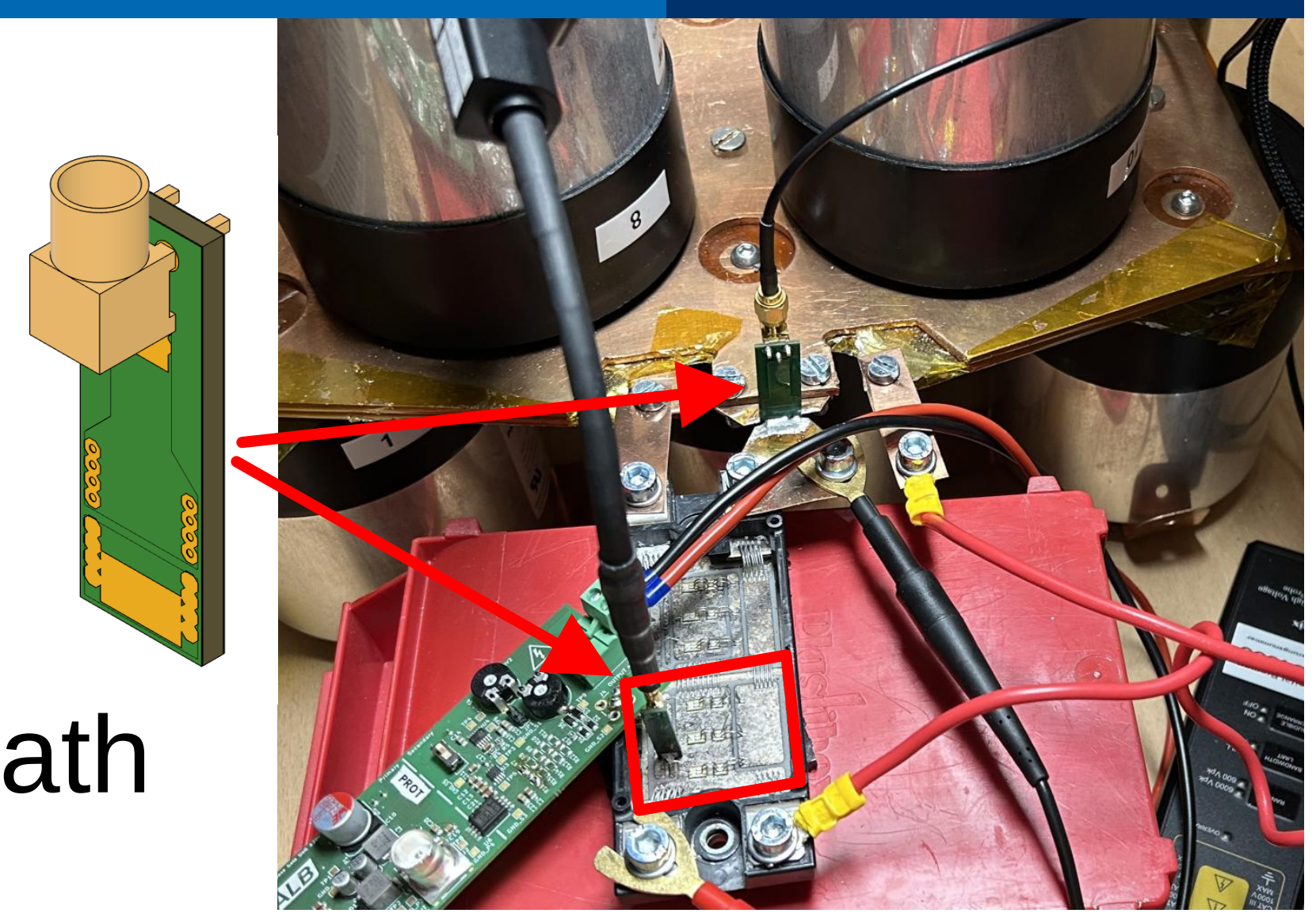
BACKGROUND

- Current asymmetries can be caused by variations in chip-level parameters or by interconnection design
- SOA and reliability can be affected
- Asymmetric current distribution can be experimentally detected by the chip's common KS path

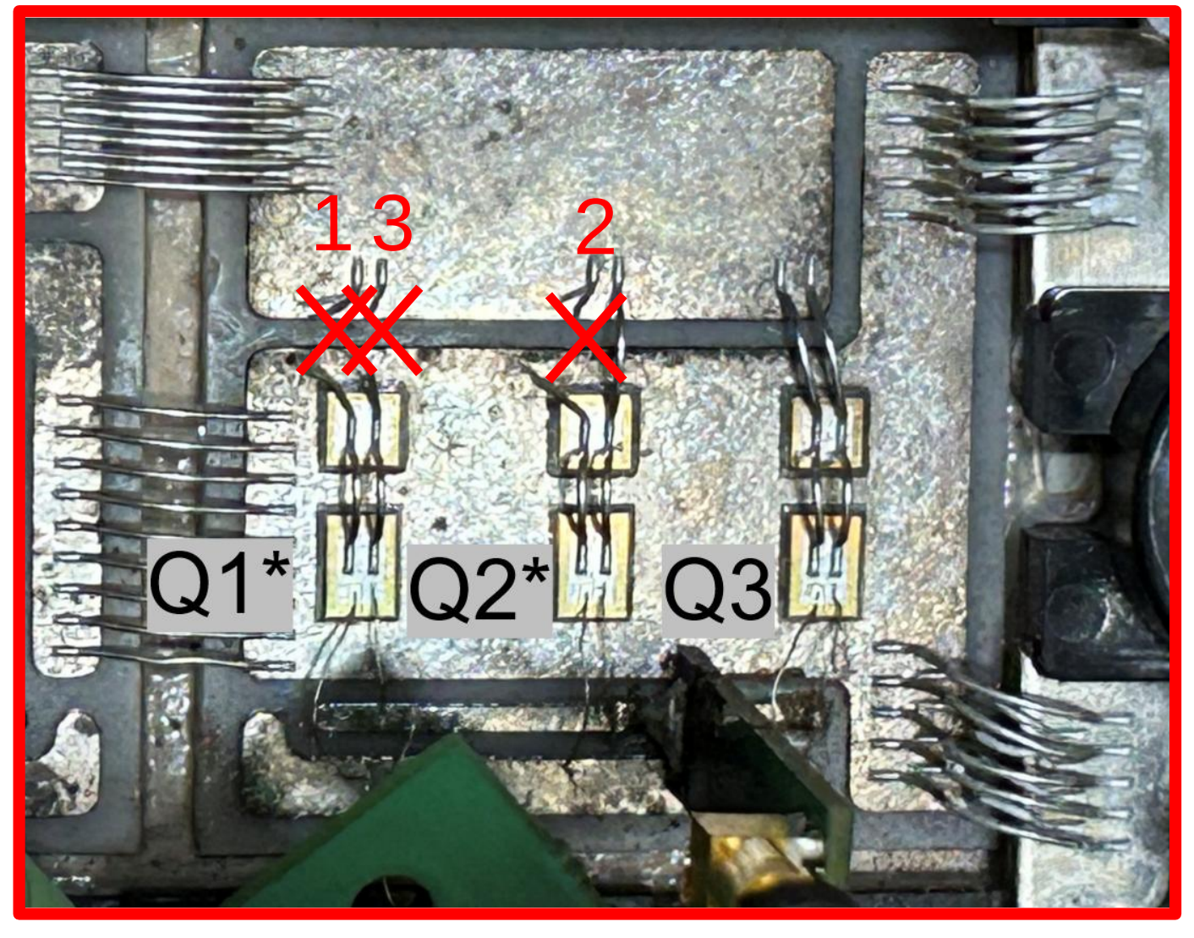
DOUBLE PULSE TEST SETUP



- **SiC-Halfbridge module** without silicone gel
- Load current detection using an M-Shunt
- Another M-Shunt as current sensor in the KS path

MEASUREMENT METHOD

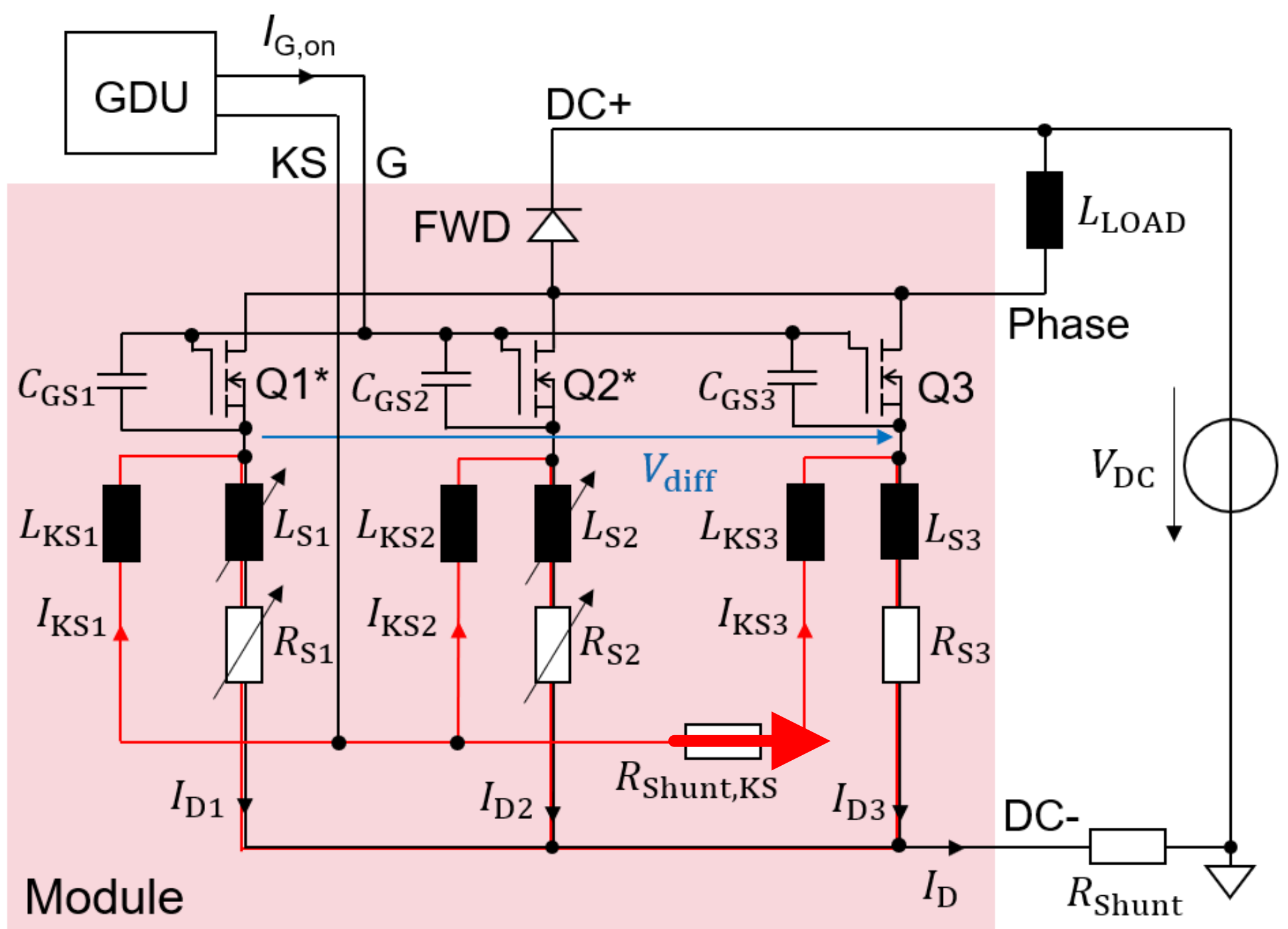
Degradation Scenario



- Initial situation of low-side switch: 3 Chips in parallel, each with 2 source BW
- BW cut sequence of chips Q1* and Q2* acc. to table
- Different sets of parasitic source impedance, up to complete disconnection

Remaining bond wires	6	5	4	3
Q1*	2	1	1	0
Q2*	2	2	1	1
Q3	2	2	2	2
Removed bond wires	0	1	2	3

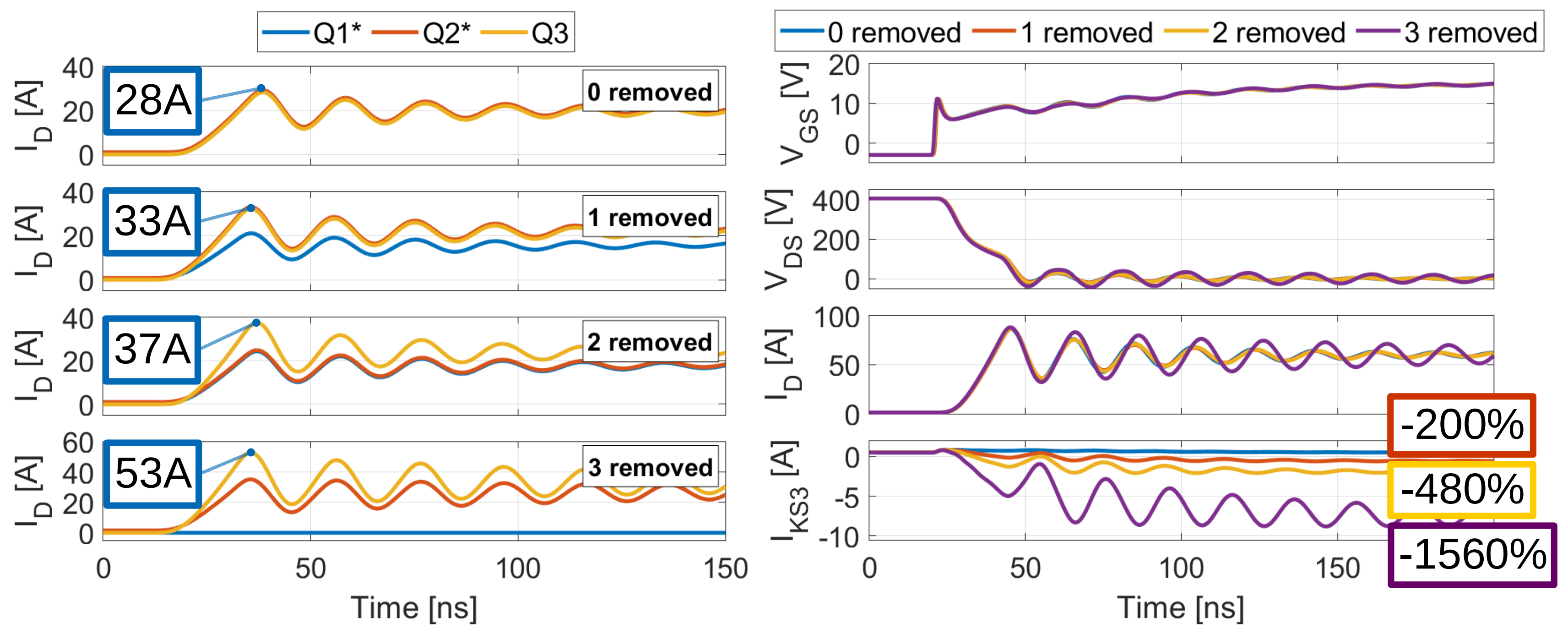
Circuit Diagram



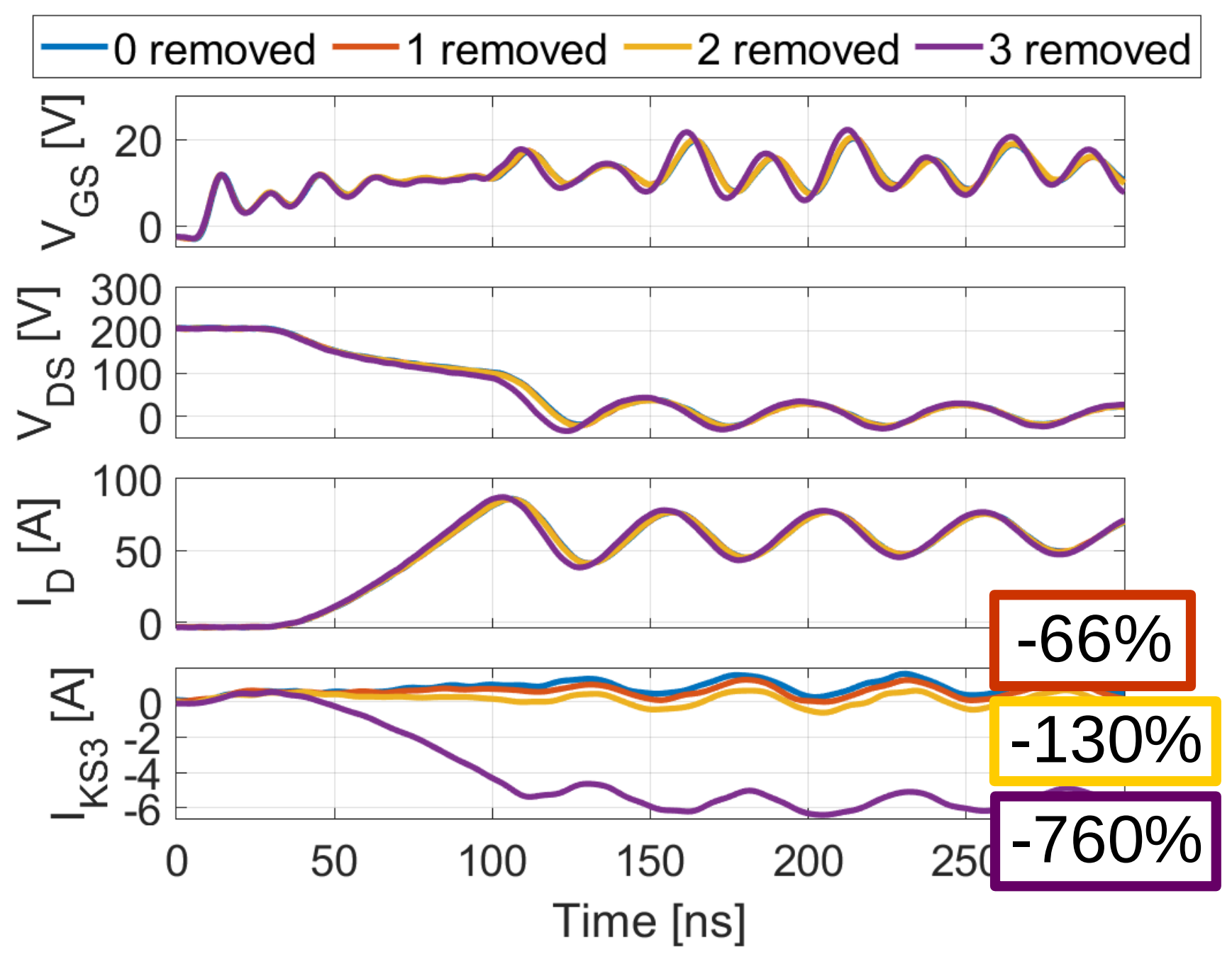
- Within the red area: Module components
- During turn-on: positive KS current peak
- Source impedance of Q1* and Q2* is increased stepwise
- Different voltage drops occur along the source connection
- Causes cross-voltage component V_{diff}
- Forces KS current from Q1* and Q2* into Q3

SWITCHING SIMULATION

- Simulation based on **3 parallel discrete devices**
- Different drain-current distribution occurs depending on source impedance
- Current through Q3 increases stepwise
- Asymmetries hardly detectable outside by V_{DS}, V_{GS} and total current
- KS current of Q3 behaves inversely compared to load current → decreases as more wires are cut



MEASUREMENT RESULTS



- Module operating point: 200V, 60A
- Changes are hardly detectable except by I_{KS}
- KS current decreases as more BW are removed
- Total chip failure of Q1* → Module still functional
- Increased stress on remaining chips Q2* and Q3
- Thermal overload of thin KS BW

CONCLUSION

- Asymmetric load current distribution within multi-chip power modules can be detected via the KS current successfully
- Viable method to detect design issues during development and even degradation in operation

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